INTEGRATED DIGITALLY CONTROLLED 6-BIT PHASE SHIFTER, 4-BIT ATTENUATOR, AND T/R SWITCH USING MULTIFUNCTION SELF ALIGNED GATE PROCESS

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Abstract

A monolithic microwave and digital integrated circuit (MMDIC) consisting of a 12-bit serial-to-parallel converter, 6-bit phase shifter, 4-bit attenuator, and SPDT switch has been designed and fabricated using the standard Multifunction Self-Aligned Gate (MSAG) process, with a full functional yield of over 27%. By combining digital circuitry with these microwave control circuits, the number of control lines is reduced from 16 to 3, allowing simplification of the subsystem architecture.

Introduction

As the performance requirements and complexity of advanced electronics systems increase, the on-chip integration of digital and microwave circuits is warranted to reduce system costs. Highly integrated GaAs ICs have been demonstrated for digital ICs containing over 10^5 FETs [1] and for microwave ICs containing over 65 mm of FET gate periphery [2]. However, little has been done to combine microwave and digital circuits on–chip at high levels of complexity. For advanced system applications in electronic warfare, communications, and radar, chips which combine digital and microwave circuit functions at high levels of complexity are badly needed for overall system simplification, increased reliability, and lower cost.

Very limited work on such monolithic microwave and digital integrated circuits (MMDICs) has been reported in the literature due to the lack of processes capable of readily combining microwave and digital functions on-chip [3], [4]. However, ITT's versatile Multifunction Self-Aligned Gate (MSAG) process is well suited for such applications. The purpose of this paper is to demonstrate the feasibility of the MSAG process for developing a complex integrated digital and microwave integrated circuit. The microwave portion of this chip chosen for this demonstration consists of a 6-bit phase shifter, a 4-bit attenuator and a single-pole double-throw (SPDT) switch. The digital circuit is a 12-bit serial-to-parallel converter which converts 12-bit serial data into a 12-bit parallel word with complementary outputs. In addition, the digital circuit accepts ECL or CMOS inputs and converts them to 0 and -3.5 V outputs to drive switching FETs used in MMICs. To the best of our knowledge, this is the first reported digital decoder combined with multiple microwave circuits in a single integrated circuit. The MMDIC reduced the interconnect bonding connections by four fold and provided a manufacturable yield for the combined circuit of over 27%.

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Circuit Design

The serial-to-parallel converter is a 12-bit time-division demultiplexer and its block diagram is shown in Fig. 1. A Johnson counter generates the internal timing signals by dividing the system clock by 12. It has automatic error correction for operation from non-valid states. The shift register consists of a chain of 12 D-type flip-flops also driven by the system clock. After the reset signal is released, demultiplexing begins and the serial word is scanned into the shift register. The counter provides the trigger signal for loading the shift register data into the hold register making the data available at the chip outputs. The digital circuit accepts a 12-bit serial CMOS input word and, after demultiplexing, converts it into twelve control lines at voltage levels

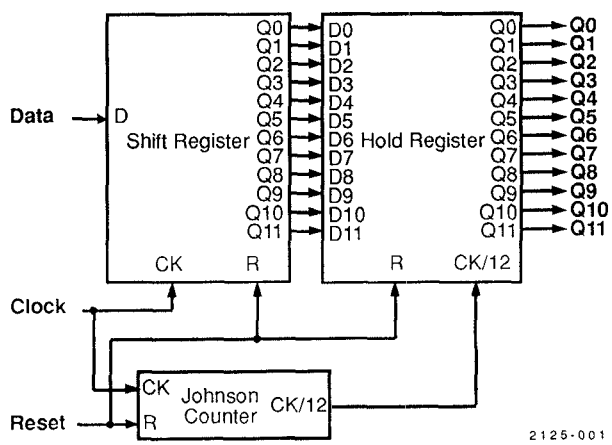

Fig. 1. Block diagram of a 12-bit serial-to-parallel converter which reduces the number of inputs from 24 to 3.

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of 0 and -3.5 V to drive MMIC switching FETs. The MSAG Enhancement/Depletion Direct Coupled FET Logic (E/D DCFL) is used to obtain high performance at low power dissipation. The serial-to-parallel converter has 243 gates and requires three inputs. It provides sixteen outputs and dissipates less than 270 mW power.

The microwave portion of the chip consists of a 6-bit phase shifter, a 4-bit attenuator and a SPDT switch. Each of these circuits uses FET switches to change states. The 6-bit phase shifter requires a single control line for each of the bits. However, each attenuator bit and the SPDT switch require two control lines carrying complementary 0/-3.5 V and -3.5/0 V signals to switch states. Therefore, without the on-chip drivers, 16 control lines would be required to drive 11 microwave functions.

The 6-bit phase shifter and SPDT switch designs use standard MSAG small-signal FETs (SFETs). The switch uses a 300-μm and a 400-μm gate width FET in a simple series - shunt configuration for each of its throws. This approach provides 20 dB of isolation and is very broadband and process tolerant. The phase shifter contains a variable phase bit, and 11.25°, 22.5°, 45°, 90° and 180° digital bits which enable it to obtain a transmission phase shift of 0 through 360 degrees with an accuracy of ± 2°. Additionally, the phase shifter is designed to have minimal amplitude variation between phase states. The variable bit and 11.25°, 22.5°, and 45° bits use a loaded-line configuration, while the 90° and 180° bits are of the reflection type. The 4-bit attenuator design contains 4 individual step attenuators, 1 dB, 2 dB, 4 dB and 8 dB, allowing amplitude control from 0 to 15 in 1-dB steps with ± 1 dB accuracy. Each step attenuator uses three FET's in a "T" structure. Because the attenuator phase shift must be minimal between the low-loss and high-loss states, inductive and resistive elements are switched in and out with the FETs to obtain a constant transmission phase.

Fabrication Process

The MMDICs are fabricated with the Multifunction Self-Aligned Gate (MSAG) process which has capability of producing multifunction ICs and can combine enhancement-mode FETs (EFETs), depletion-mode FETs (DFETs), small-signal FETs (SFETs), power FETs (PFETs) and switching FETs (SWFETs) on the same chip. The MSAG fabrication process is illustrated in Fig. 2. The device active regions are defined by selective ion implantation, with a Si active layer implant and a Mg buried-p implant. The titanium tungsten nitride refractory gate metal is deposited by sputtering and patterned into "T-gate" structures using a Ni etch mask and reactive-ion etching. The gate length is 0.4 μm. A photoresist stripe along the gate is employed to improve the breakdown voltage of the FETs as appropriate. Microwave FETs for small-signal or power amplification use the asymmetrically placed stripe on the drain side of the gate shown in Fig. 2. Switching FETs employ a symmetrically placed resist stripe for symmetrical device characteristics with high breakdown voltages. Digital EFETs and DFETs omit the photoresist stripe entirely, to provide symmetrical devices with lower parasitic resistances. To reduce these parasitics even further, the digital FETs also require a self-aligned n' implant performed after the Ni gate etch mask has been removed. After annealing, the GaAs surface is passivated with silicon nitride, which is planarized and etched back to expose the gate, permitting overlay metal contact for reduced gate resistance. First-level metal is used for three functions: to overlay the gate, to form interconnections, and as a capacitor bottom plate. Gold plating 4.5-μm thick is used for digital circuit second-level interconnections, air bridge cross-overs, bonding pads, and capacitor top plates. The process also includes through-wafer etched via holes, with a final wafer thickness of 125 μm. A photomicrograph of the combined digital and the microwave circuit is illustrated in Fig. 3. Wafer averaged dc parameters for FETs used in this MMDIC are given in Table 1.

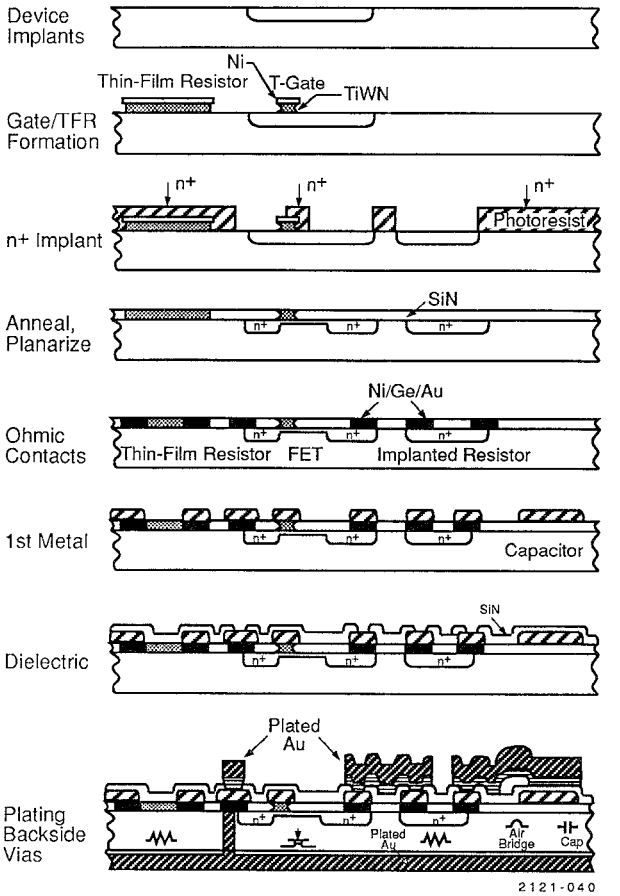


Fig. 2. Multifunction Self-Aligned Gate Fabrication Process.

MMDIC Performance

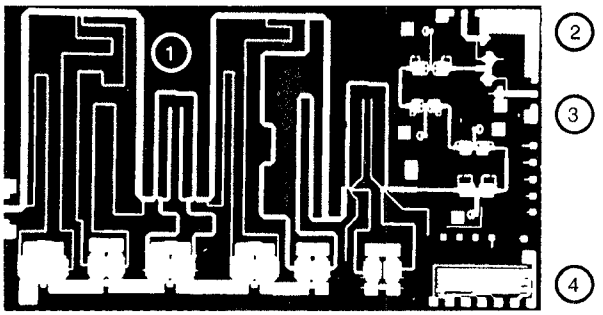
Testing the digital decoder requires that all edges be synchronized to ensure correct loading and shifting of the data. Fig. 4 shows the clock frequency operating at 50 MHz, with the data at the Nyquist rate of 25 MHz. The circuit is designed to clock up to 200 MHz,

Table 1

Wafer-Averaged DC Parameters

Parameter	EFET	DFET	SFET	PFET
V_T (V)	0.15	-0.46	-0.85	-2.95
I_{DSS} (mA/mm)	73	48	147	308
g_m (mS/mm)	314	193	210	132

but the test equipment used imposes a 50 MHz upper limit. Furthermore, Fig. 4 also shows the reset, hold enable, Q10, and Q11 signals. The decoder is activated when the "reset" goes low, which causes valid data to be loaded into the shift register. This continues for 12 clock cycles, at which time the Johnson counter times out and causes "hold enable" to go low and the outputs in the hold register become valid. Therefore, all the odd outputs (Q1, Q3, . . ., Q11) should go high and all even outputs should go low for at least



1. 6-bit Phase Shifter
2. SPDT Switch
3. 4-bit Attenuator
4. Digital Controller

Fig. 3. Photomicrograph of a combined microwave and digital circuit. This integrates 837 EFETs and DFETs, 28 SFETs and PFETs, 66 Schottky diodes, and 28 resistors. The total chip size is 9.8 x 5.4 mm^2.

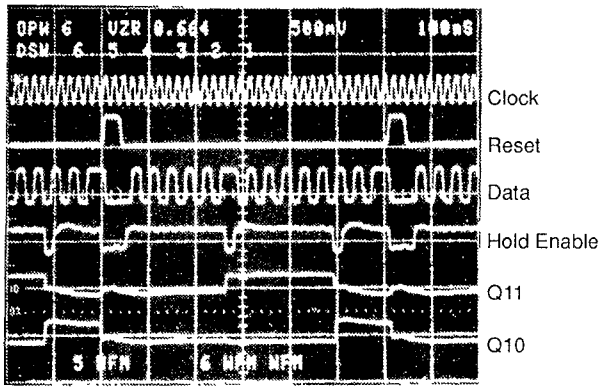


Fig. 4. Functionality of the digital decoder is shown operating at the equipment-limited clock rate of 50 MHz and data rate of 25 MHz.

12 clock cycles as shown in the figure. However, on the 13th clock cycle from the first reset the data is altered 180 degrees, to cause the odd outputs to go low and the even outputs to go high to verify they switch. The data input uses a 32-bit word from the word generator that generates a reset on clock cycle number 32. Hence, as shown in the figure, the outputs go to their new state for only six clock cycles.

Once the digital decoder functionality was verified the entire MMDIC was tested by clocking the proper serial word into the serial-to-parallel converter and observing the microwave circuit functionality. Fig. 5 shows the measured phase shift for each of the individual bits relative to a zero-phase reference over a 5.5 to 6.5 GHz frequency range. Each of the bits gives the desired phase shift within 10% of nominal value. As illustrated in Fig. 6 the amplitude variation associated with each bit does not exceed ±1 dB. Fig. 7 shows the attenuator's measured 4-state attenuation performance. Every bit gives its nominal amplitude value within

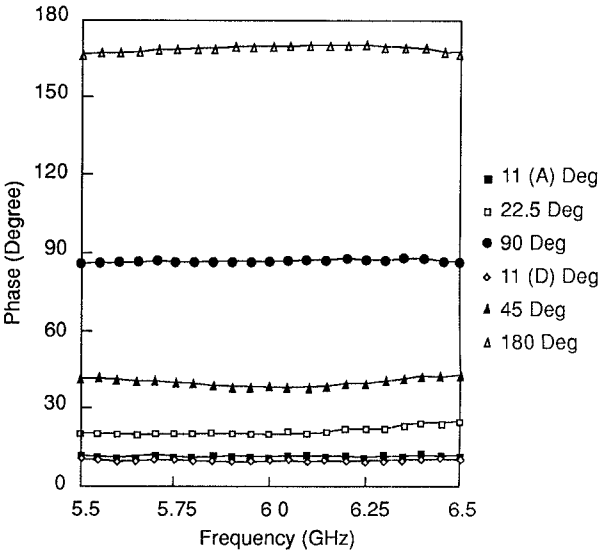


Fig. 5. The phase shift of each of the 6 bits as referenced to the zero degree state. All bits give this nominal phase shift within a 10% tolerance window.

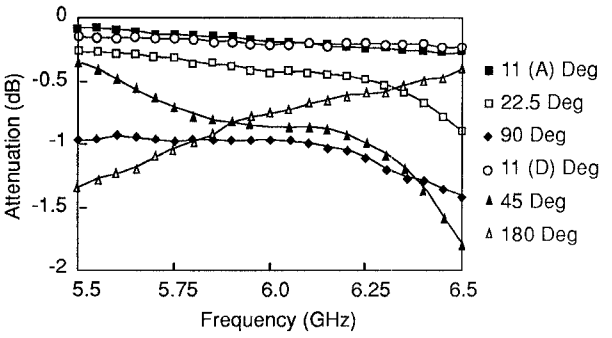


Fig. 6. The amplitude variation associated with each at the 6 phase shifter bits referenced to the zero degree state. The worst-case variation (45 degree bit) is less than -2 dB.

0.5 dB. The associated phase shift is shown in Fig. 8 and the worst-case phase shift for any attenuator state is 8 degrees. The measured insertion loss and isolation for the SPDT switch were better than 2 dB and 20 dB, respectively. The MMDIC performance is summarized in Table 2.

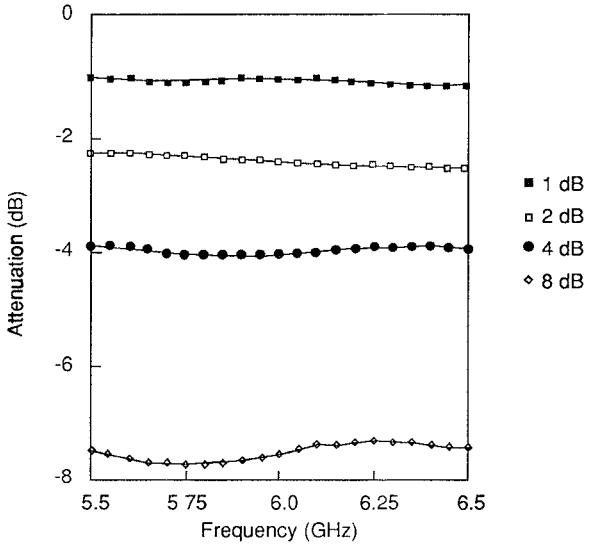


Fig. 7. The amplitude performance of the 4-bit attenuator. Each bit exhibits its nominal values with less than 0.5 dB of error. The error in the 1 dB and 4 dB bits is almost imperceptible.

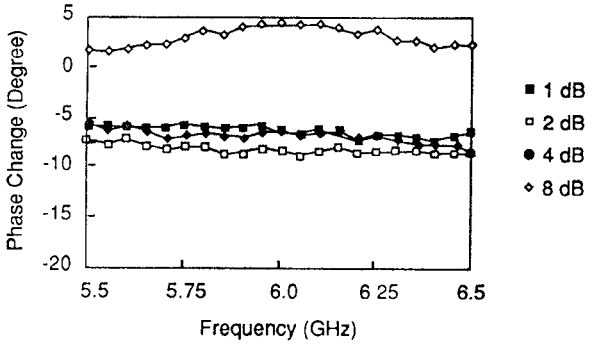


Fig. 8. The phase change associated with each of the 4 attenuator bits as referenced to the zero dB attenuation state. The 1, 2, and 4 dB states exhibit -6 to -8 degree phase change and the 8 dB states shows up to a +5 degrees at phase change.

Conclusions

A combined digital and microwave IC consisting of a 6-bit phase shifter, a 4-bit attenuator and a SPDT switch, all controlled on-chip by a 12-bit serial-to-parallel converter, has been successfully designed and fabricated using ITT's Multifunction Self-Aligned Gate process. The complex MMDIC was tested on wafer with a yield of over 27% for fully functional ICs. The on-chip combination of multiple circuit functions, including both digital and microwave, not only simplifies the bonding connections, but also reduces the subsystem cost, and increases its reliability.

Table 2

Performance of Monolithic Microwave and Digital Integrated Circuit

Circuit Parameter	Designed	Measured
6-bit Phase Shifter		
Frequency (GHz)	5.5 to 6.5	5.5 to 6.5
Phase Range (degree)	0-360	0-350
Insertion Loss, max (dB)	10	10
Return Loss, max (dB)	12	13
Amplitude Flatness per bit (dB)	±0.5	±1
4-bit Attenuator		
Frequency (GHz)	5.5 to 6.5	5.5 to 6.5
Attenuation Range (dB)	0-15	0-15
Max. Phase Shift/bit (degree)	±5	±8
Insertion Loss (dB)	2	2
Return Loss (dB)	16	13
SPDT Switch		
Frequency (GHz)	5.5 to 6.5	5.5 to 6.5
Insertion Loss, max (dB)	1.5	1.5
Isolation, min (dB)	20	22
Return Loss, min (dB)	14	15
12-bit Serial-to-Parallel Converter		
Clock Rate (MHz)	200	50*
Power Dissipation (mW)	270	240
MMDIC Yield (%)		27

*Limited by test equipment

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